SAMSUNG

Practical Implementation of Active Mode Power Gating Circuits

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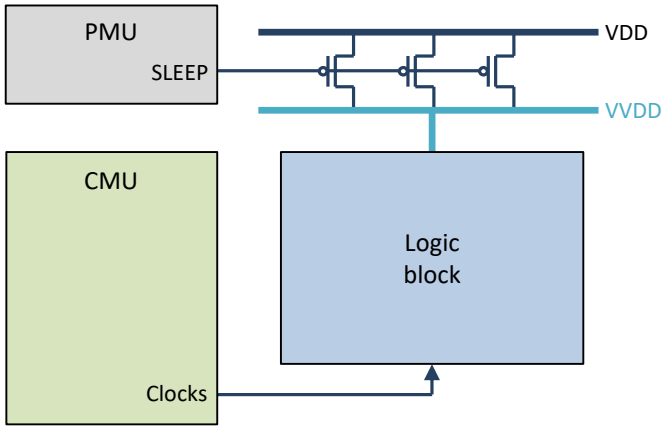
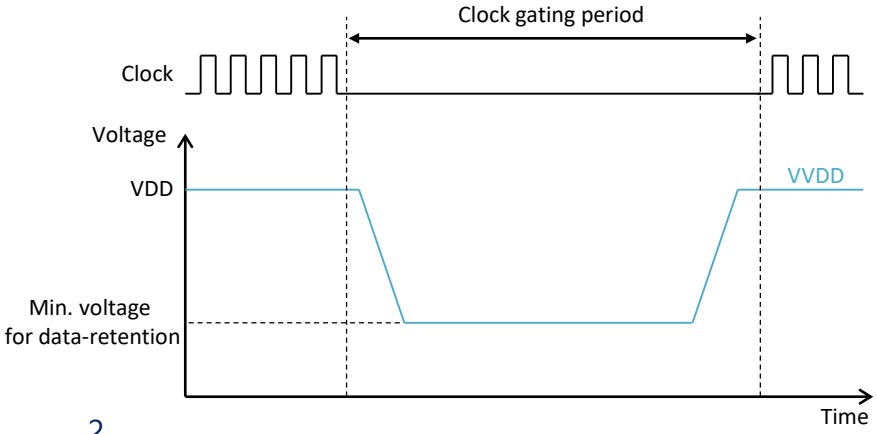
Motivation

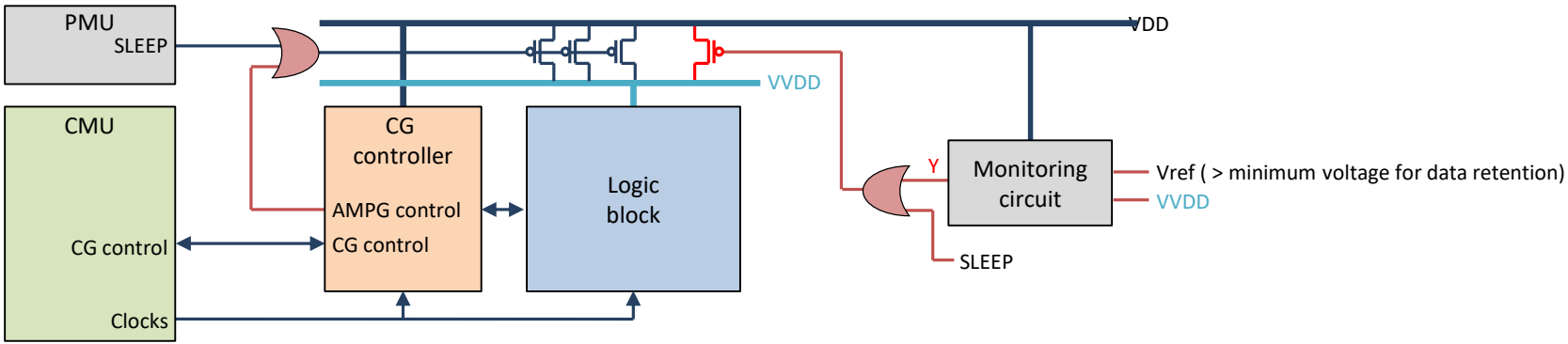
- **Active mode power gating**
  - **Combination of clock gating and power gating**
    - Lowering virtual VDD (VVDD) to reduce active mode leakage current while (block-level) clock gating is applied
  - **The most effective run-time technique to reduce active mode leakage current**
- **Design challenges**
  - **How to lower VVDD level during clock gating period**
    - VVDD must be higher than the minimum guaranteed voltage for data-retention
  - **VVDD must be fully charged before releasing from clock gating**
  - **Care of wake-up noise and wake-up time**





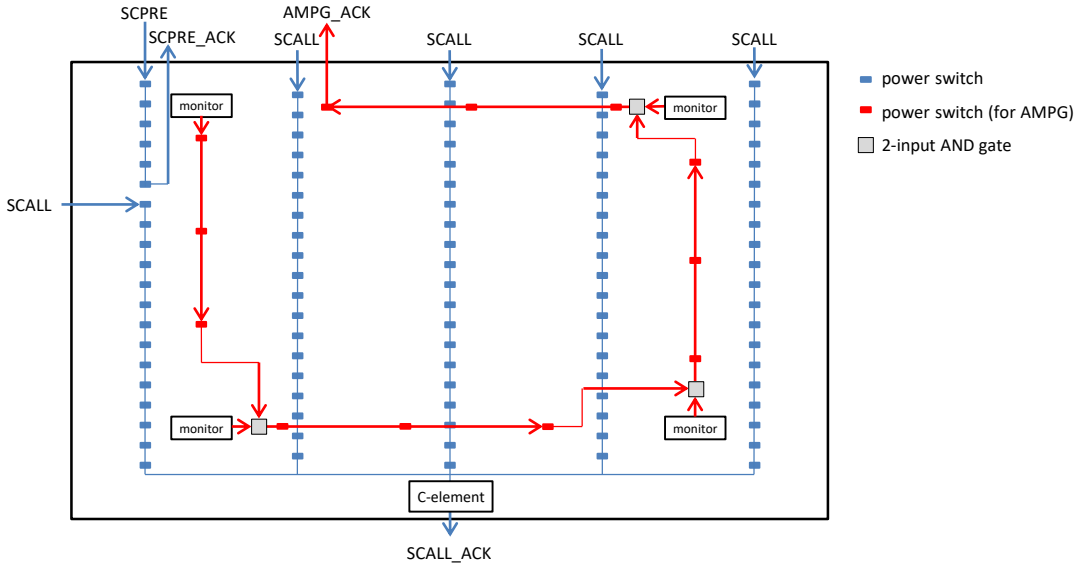
Main Idea

- **Employ (fully digital) voltage monitoring circuit and small number of power switches to control VVDD**
  - **All the existing power switches are turned off during active mode power gating**
  - **If VVDD is lower than Vref, dedicated power switches are turned on (Y = 0), so that VVDD is charged**
    - Vref can be tuned by user
  - **Otherwise, dedicated power switches are also turned off (Y = 1)**
- **Utilize the existing block-led clock gating scheme**
  - **Block can request to apply or release clock gating, and also deny the request of CMU to apply or release clock gating**
    - Release request is forwarded to CMU after VVDD is fully charged



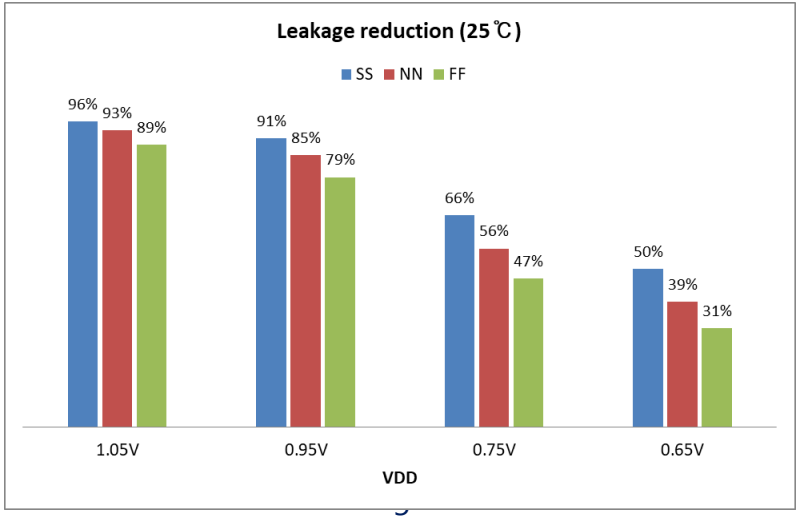
Main Idea

- **Wake-up time should be as small as possible to reduce "timing overhead of AMPG"**
  - SLEEP signal is propagated in daisy chain fashion, and each signal drives multiple power switches
- **Wake-up noise of AMPG is smaller than that of normal power gating**
  - The number of dedicated power switches is smaller than that of "PRE-group" power switches
  - VVDD is charged from minimum voltage for data-retention to VDD



Simulation Result

- **Experimental setup**
  - Samsung 10-nm technology / test circuit: 5 industrial circuits
  - Minimum voltage for data-retention is assumed as 0.475V
  - SPICE simulation was performed using gate-level netlists of each circuit and monitoring circuit
- **Experimental result**
  - Compared to clock-gated circuit, leakage current is reduced by 89% and 31% when VDD is set to 1.05V and 0.65V respectively
  - Overhead of monitoring circuit is negligible



Summary

- **Active mode power gating**
  - The most effective run-time technique to reduce active mode leakage current
  - We first employ active mode power gating to commercial design
- **Our approach to resolve design challenges**
  - Employ (fully digital) voltage monitoring circuit to control VVDD level
  - Utilize existing block-led clock gating scheme
  - Special care of wake-up time and wake- noise
- **Simulation result**
  - Leakage current can be reduced by more than 89% compared to clock-gated circuit (when VDD = 1.05V and temperature = 25℃)